WHAT IS CLAIMED IS:

1. A capacitor comprising:

a strained semiconductor layer;

a bottom electrode formed in a portion of the strained semiconductor layer;

a capacitor dielectric overlying the bottom electrode;

a top electrode overlying the capacitor dielectric; and

at least one bottom electrode contact region formed in the strained semiconductor layer adjacent the bottom electrode, the at least one bottom electrode contact region being doped to a first conductivity type wherein the bottom electrode is operationally the first conductivity type.

2. The capacitor of claim 1 wherein the capacitor is a decoupling capacitor.

3. The capacitor of claim 2 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

4. The capacitor of claim 2 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

5. The capacitor of claim 1 wherein the bottom electrode is substantially flat.

6. The capacitor of claim 1 further comprising an isolation region adjacent to bottom electrode.

7. The capacitor of claim 6 wherein the isolation region is shallow trench isolation.

8. The capacitor of claim 1 wherein the top electrode is substantially flat.

9. The capacitor of claim 1 wherein the strained semiconductor layer comprises a strained silicon layer.

10. The capacitor of claim 9 and further comprising a silicon germanium layer underlying the strained silicon layer.

11. The capacitor of claim 10 wherein the silicon germanium layer has a germanium concentration in the range of about 10 to about 90%.

12. The capacitor of claim 11 wherein the silicon germanium layer has a germanium concentration in the range of about 20 to about 40%.

13. The capacitor of claim 1 wherein the semiconductor layer comprises of silicon and germanium.

14. The capacitor of claim 1 and further comprising an insulator layer underlying the strained semiconductor layer.

15. The capacitor of claim 14 wherein the insulator layer comprises silicon oxide.

16. The capacitor of claim 14 wherein the insulator layer has a thickness of less than about 1200 angstroms.

17. The capacitor of claim 14 wherein the bottom electrode is isolated from adjacent elements by mesa isolation.

18. The capacitor of claim 14 wherein the semiconductor layer has a thickness in the range of about 20 angstroms to about 500 angstroms.

19. The capacitor of claim 1 wherein the top electrode comprises a material selected from the group consisting of poly-crystalline silicon and poly-crystalline silicon-germanium.

20. The capacitor of claim 1 wherein the top electrode comprises a material selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

21. The capacitor of claim 1 wherein the top electrode comprises a material selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations thereof.

22. The capacitor of claim 1 wherein the top electrode comprises a material selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, and combinations thereof.

23. The capacitor of claim 1 wherein the top electrode comprises a material selected from the group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

24. The capacitor of claim 1 wherein the capacitor dielectric comprises a high permittivity dielectric.

25. The capacitor of claim 24 wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

26. The capacitor of claim 24 wherein the high permittivity dielectric has a relative permittivity of larger than about 10.

27. The capacitor of claim 24 wherein the high permittivity dielectric has a relative permittivity of larger than about 20.

28. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of smaller than about 10 angstroms.

29. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of smaller than about 50 angstroms.

30. The capacitor of claim 1 wherein the capacitor dielectric has a physical thickness of smaller than about 100 angstroms.

31. The capacitor of claim 1 wherein the capacitor has a width of larger than about 5 microns.

32. The capacitor of claim 1 wherein the capacitor has a width of larger than about 10 microns.

33. The capacitor of claim 1 wherein the capacitor has a length of larger than about 1 micron.

34. The capacitor of claim 1 wherein the capacitor has a length of larger than about 5 microns.

35. The capacitor of claim 1 wherein the bottom electrode is physically doped to a first conductivity type and the bottom electrode contact region is physically doped to a second conductivity type.

36. The capacitor of claim 35 wherein the first conductivity type is n-type and the second conductivity type is p-type.

37. The capacitor of claim 35 wherein the first conductivity type is p-type and the second conductivity type is n-type.

38. The capacitor of claim 1 wherein the bottom electrode is physically doped to a first conductivity type and the bottom electrode contact region is physically doped to the first conductivity type.

39. The capacitor of claim 1 and further comprising spacers formed on the sides of the top electrode.

40. The capacitor of claim 39 wherein the spacers comprise silicon nitride.

41. The capacitor of claim 39 and further comprising an etch-stop layer overlying the top electrode and the spacers.

42. The capacitor of claim 41 wherein the etch-stop layer comprises silicon nitride.

43. The capacitor of claim 41 and further comprising an inter-layer dielectric overlying the etch-stop layer.

44. The capacitor of claim 43 wherein the inter-layer dielectric comprises silicon oxide.

45. The capacitor of claim 43 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.5.

46. The capacitor of claim 43 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.0.

47. The capacitor of claim 43 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

48. The capacitor of claim 43 further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

49. A decoupling capacitor comprising:

a semiconductor substrate including a strained silicon layer,

a substantially flat bottom electrode formed in a portion of the strained silicon layer;

a capacitor dielectric overlying the bottom electrode;

a substantially flat top electrode overlying said capacitor dielectric;

wherein the top electrode is connected to a first reference voltage line and the bottom electrode is connected to a second reference voltage line.

50. The capacitor of claim 49 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

51. The capacitor of claim 49 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

52. The capacitor of claim 49 wherein the semiconductor substrate further comprises a silicon germanium layer underlying the strained silicon layer.

53. The capacitor of claim 49 wherein the semiconductor substrate further comprises an insulator layer underlying the strained silicon layer.

54. The capacitor of claim 49 wherein the top electrode comprises a material selected from the group consisting of poly-crystalline silicon and poly-crystalline silicon-germanium.

55. The capacitor of claim 49 wherein the top electrode comprises a material selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

56. The capacitor of claim 49 wherein the top electrode comprises a material selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations thereof.

57. The capacitor of claim 49 wherein the top electrode comprises a material selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

58. The capacitor of claim 49 wherein the top electrode comprises a material selected from the group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

59. The capacitor of claim 49 wherein the capacitor dielectric comprises a high permittivity dielectric.

60. The capacitor of claim 59 wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

61. The capacitor of claim 59 wherein the high permittivity dielectric has a relative permittivity of larger than about 10.

62. The capacitor of claim 59 wherein the high permittivity dielectric has a relative permittivity of larger than about 20.

63. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of smaller than about 10 angstroms.

64. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of smaller than about 50 angstroms.

65. The capacitor of claim 59 wherein the capacitor dielectric has a physical thickness of smaller than about 100 angstroms.

66. The capacitor of claim 49 wherein the capacitor has a width of larger than about 5 microns.

67. The capacitor of claim 49 wherein the capacitor has a width of larger than about 10 microns.

68. The capacitor of claim 49 wherein the capacitor has a length of larger than about 1 micron.

69. The capacitor of claim 49 wherein the capacitor has a length of larger than about 5 microns.

70. The capacitor of claim 49 wherein the bottom electrode has a first conductivity type and wherein the capacitor further comprises at least one doped region of a second conductivity type located within the strained silicon layer adjacent the bottom electrode.

71. The capacitor of claim 70 wherein the first conductivity type is n-type and the second conductivity type is p-type.

72. The capacitor of claim 70 wherein the first conductivity type is p-type and the second conductivity type is n-type.

73. The capacitor of claim 49 wherein the bottom electrode has a first conductivity type and wherein the capacitor further comprises at least one doped region of the first conductivity type located with the strained silicon layer adjacent the bottom electrode.

74. The capacitor of claim 49 and further comprising an etch-stop layer overlying the top electrode.

75. The capacitor of claim 74 wherein the etch-stop layer comprises silicon nitride.

76. The capacitor of claim 74 and further comprising an inter-layer dielectric overlying the etch-stop layer, wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.5.

77. The capacitor of claim 76 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.0.

78. The capacitor of claim 76 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

79. The capacitor of claim 76 further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

80. The capacitor of claim 49 further comprising a shallow trench isolation region adjacent to bottom electrode.

81. The capacitor of claim 49 wherein the bottom electrode is isolated by mesa isolation.

82. A method of forming a capacitor, the method comprising:

providing a semiconductor substrate including a strained silicon layer;

forming a bottom electrode in the strained silicon layer;

forming a capacitor dielectric on bottom electrode;

forming a top electrode on capacitor dielectric;

forming a bottom electrode contact region within the strained silicon layer adjacent the bottom electrode; and

electrically connecting the bottom electrode and the bottom electrode contact region.

83. The method of claim 82 wherein the capacitor is a decoupling capacitor, the method further comprising connecting the bottom electrode to a first reference node and connecting the top electrode to a second reference node.

84. The method of claim 82 wherein forming the bottom electrode comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region to form a bottom electrode.

85. The method of claim 84 wherein the active region has a doping concentration of larger than about 10^{19} cm^{-3}.

86. The method of claim 82 wherein forming the capacitor dielectric comprises a chemical vapor deposition step or sputter deposition step.

87. The method of claim 82 wherein the step of forming the capacitor dielectric comprises:

forming an interfacial oxide layer; and

forming a high permittivity dielectric layer.

88. The method of claim 82 wherein forming bottom electrode contact region comprises:

doping a portion of the strained silicon layer not covered by top electrode;

forming spacers on sides of the top electrode; and

doping a portion of the silicon layer not covered by the top electrode and spacers.

89. The method of claim 88 wherein the spacers comprise silicon nitride.

90. The method of claim 88 further comprising:

depositing an etch-stop layer over top electrode and spacers;

forming an inter-layer dielectric over etch-stop layer;

forming contact holes in inter-layer dielectric; and

filling the contact holes with a conductive material to form contact plugs.

91. The method of claim 90 wherein the etch-stop layer comprises silicon nitride.

92. The method of claim 90 wherein the inter-layer dielectric comprises silicon oxide.

93. The method of claim 90 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.5.

94. The method of claim 90 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity smaller than about 3.0.

95. The method of claim 90 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

96. The method of claim 90 wherein filling the contact holes comprises forming a first contact plug that electrically contacts the bottom electrode and forming a second contact plug that electrically contacts the top electrode.

97. The method of claim 96 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.

98. The method of claim 96 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

99. The method of claim 82 wherein the semiconductor substrate further comprises a silicon germanium layer underlying the strained silicon layer.

100. The method of claim 99 wherein the silicon germanium layer has a germanium concentration in the range of about 10 to about 90%.

101. The method of claim 99 wherein the silicon germanium layer has a germanium concentration in the range of about 20 to about 40%.

102. The method of claim 82 wherein the semiconductor substrate further comprises an insulator layer underlying the strained silicon layer.

103. The method of claim 102 wherein the insulator layer comprises silicon oxide.

104. The method of claim 102 wherein the insulator layer has a thickness of less than about 1200 angstroms.

105. The method of claim 82 wherein the strained silicon layer has a thickness in the range of about 20 angstroms to about 500 angstroms.

106. The method of claim 82 wherein the top electrode comprises poly-crystalline silicon or poly-crystalline silicon-germanium.

107. The method of claim 82 wherein the top electrode is selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

108. The method of claim 82 wherein the top electrode is selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations thereof.

109. The method of claim 82 wherein the top electrode is selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, and combinations thereof.

110. The method of claim 82 wherein the top electrode is selected from the group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

111. The method of claim 82 wherein the capacitor dielectric comprises a high permittivity dielectric.

112. The method of claim 111 wherein the high permittivity dielectric is selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

113. The method of claim 111 wherein the high permittivity dielectric has a relative permittivity of larger than about 10.

114. The method of claim 111 wherein the high permittivity dielectric has a relative permittivity of larger than about 20.

115. The method of claim 82 wherein the capacitor dielectric has a physical thickness of smaller than about 10 angstroms.

116. The method of claim 82 wherein the capacitor dielectric has a physical thickness of smaller than about 50 angstroms.

117. The method of claim 82 wherein the capacitor dielectric has a physical thickness of smaller than about 100 angstroms.

118. The method of claim 82 wherein the capacitor has a width of larger than about 5 microns.

119. The method of claim 82 wherein the capacitor has a width of larger than about 10 microns.

120. The method of claim 82 wherein the capacitor has a length of larger than about 1 micron.

121. The method of claim 82 wherein the capacitor has a length of larger than about 5 microns